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Declaration and Power of Attorney For Patent Application

Erklärung Für Patentanmeldungen Mit Vollmacht

German Language Declaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

As a below named inventor, I hereby declare that:

dass mein Wohnsitz, meine Postanschrift, und meine Staatsangehörigkeit den im Nachstehenden nach meinem Namen aufgeführten Angaben entsprechen,

My residence, post office address and citizenship are as stated below next to my name,

dass ich, nach bestem Wissen der ursprüngliche, erste und alleinige Erfinder (falls nachstehend nur ein Name angegeben ist) oder ein ursprünglicher, erster und Miterfinder (falls nachstehend mehrere Namen aufgeführt sind) des Gegenstandes bin, für den dieser Antrag gestellt wird und für den ein Patent beantragt wird für die Erfindung mit dem Titel:

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Method of Producing a Micro-Electromechanical Element

deren Beschreibung

(zutreffendes ankreuzen)

☐ hier beigefügt ist.

☐ am _____ unter der Anmeldungsseriennummer _____ eingereicht wurde und am _____ abgeändert wurde (falls tatsächlich abgeändert).

the specification of which

(check one)

is attached hereto.

☒ was filed on 6/12/01 as Application Serial No. 09/868,156 and was amended on _____ (if applicable)

Ich bestätige hiermit, dass ich den Inhalt der obigen Patentanmeldung einschliesslich der Ansprüche durchgesehen und verstanden habe, die eventuell durch einen Zusatzantrag wie oben erwähnt abgeändert wurde.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

Ich erkenne meine Pflicht zur Offenbarung irgendwelcher Informationen, die für die Prüfung der vorliegenden Anmeldung in Einklang mit Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) von Wichtigkeit sind, an.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

Ich beanspruche hiermit ausländische Prioritätsvorteile gemäss Abschnitt 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 119 aller unten angegebenen Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde, und habe auch alle Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde nachstehend gekennzeichnet, die ein Anmeldedatum haben, das vor dem Anmeldedatum der Anmeldung liegt, für die Priorität beansprucht wird.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

German Language Declaration

- Prior foreign applications
  Priorität beansprucht

			Priority Claimed	
19857741.9 (Number) (Nummer)	Germany (Country) (Land)	15/12/98 (December 15, 1998) (Day/Month/Year Filed) (Tag/Monat/Jahr eingereicht)	[X] Yes Ja	[ ] No Nein
19927970.5 (Number) (Nummer)	Germany (Country) (Land)	18/06/99 (June 18, 1999) (Day/Month/Year Filed) (Tag/Monat/Jahr eingereicht)	[X] Yes Ja	[ ] No Nein
PCT/EP99/07204 (Number) (Nummer)	Germany (Country) (Land)	29/09/99 (September 29, 1999) (Day/Month/Year Filed) (Tag/Monat/Jahr eingereicht)	[X] Yes Ja	[ ] No Nein

Ich beanspruche hiermit gemäss Absatz 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 120, den Vorzug aller unten aufgeführten Anmeldungen und falls der Gegenstand aus jedem Anspruch dieser Anmeldung nicht in einer früheren amerikanischen Patentanmeldung laut dem ersten Paragraphen des Absatzes 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 112 offenbart ist, erkenne ich gemäss Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) meine Pflicht zur Offenbarung von Informationen an, die zwischen dem Anmeldedatum der früheren Anmeldung und dem nationalen oder PCT internationalen Anmeldedatum dieser Anmeldung bekannt geworden sind.

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.) (Anmeldeseriennummer)	(Filing Date) (Anmeldedatum)	(Status) (patentiert, anhängig, aufgegeben)	(Status) (patented, pending, abandoned)
(Application Serial No.) (Anmeldeseriennummer)	(Filing Date) (Anmeldedatum)	(Status) (patentiert, anhängig, aufgegeben)	(Status) (patented, pending, abandoned)

Ich erkläre hiermit, dass alle von mir in der vorliegenden Erklärung gemachten Angaben nach meinem besten Wissen und Gewissen der vollen Wahrheit entsprechen, und dass ich diese eidesstattliche Erklärung in Kenntnis dessen abgebe, dass wissentlich und vorsätzlich falsche Angaben gemäss Paragraph 1001, Absatz 18 der Zivilprozessordnung der Vereinigten Staaten von Amerika mit Geldstrafe belegt und/oder Gefängnis bestraft werden koennen, und dass derartig wissentlich und vorsätzlich falsche Angaben die Gültigkeit der vorliegenden Patentanmeldung oder eines darauf erteilten Patentes gefährden können.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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German Language Declaration

VERTRETUNGSVOLLMACHT: Als benannter Erfinder beauftrage ich hiermit den nachstehend benannten Patentanwalt (oder die nachstehend benannten Patentanwälte) und/oder Patent-Agenten mit der Verfolgung der vorliegenden Patentanmeldung sowie mit der Abwicklung aller damit verbundenen Geschäfte vor dem Patent-und Warenzeichenamt: *(Name und Registrationsnummer anführen)*

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

Michael A. GLENN, Reg. No. 30,176

Donald M. HENDRICKS, Reg. No. 40,355

Kirk D. WONG, Reg. No. 43,284

Earle W. JENNINGS, Reg. No. 44,804

Christopher PEIL, Reg. No. 45,005

Telefongespräche bitte richten an: *(Name und Telefonnummer)*

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Postanschrift:

Send Correspondence to:
GLENN PATENT GROUP
3475 Edison Way, Suite L,
Menlo Park, CA 94025
U.S.A.

Voller Name des einzigen oder ursprünglichen Erfinders:	Full name of sole or first inventor NEUMEIER, Karl
Unterschrift des Erfinders Datum	Inventor's signature Date June 08, 2001
Wohnsitz	Residence Unterhaching, Germany
Staatsangehörigkeit	Citizenship German
Postanschrift	Post Office Address Muenchener Strasse 111
	D-82008 Unterhaching
Voller Name des zweiten Miterfinders (falls zutreffend)	Full name of second joint inventor, if any BOLLMANN, Dieter
Unterschrift des Erfinders Datum	Second Inventor's signature Date June 08, 2001
Wohnsitz	Residence Muenchen, Germany
Staatsangehörigkeit	Citizenship German
Postanschrift	Post Office Address Solothurner Strasse 5
	D-81475 Muenchen

(Bitte entsprechende Informationen und Unterschriften im Falle von dritten und weiteren Miterfindern angeben).

(Supply similar information and signature for third and subsequent joint inventors.)

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ASSIGNMENT

In consideration of the sum of one dollar ($ 1,00) and other good and valuable considerations paid to the undersigned, the undersigned, NEUMEIER, Karl; BOLLMANN, Dieter; agree to assign, and hereby does assign, transfer and set over to

FRAUNHOFER-GESELLSCHAFT ZUR FOERDERUNG
DER ANGEWANDTEN FORSCHUNG E.V.
located at Leonrodstrasse 54, 80636 Muenchen, Germany

(hereinafter designated as the Assignee) the entire right, title and interest for the United States, its territories, dependencies and possessions, in the invention, and all applications for patent and any Letters Patent which may be granted therefore, known as

Method of Producing a Micro-Electromechanical Element
U.S. Serial No. 09/868,156 filed 6/12/01

for which the undersigned has (have) executed an application for patent in the United States of America on .....

1) The undersigned agree to execute all papers necessary in connection with the application and any continuing of divisional or reissue applications thereof and also to execute separate assignments in connection with such applications as the Assignee may deem necessary or expedient or essential to its full protection and title in and to the invention hereby transferred.

2) The undersigned agree to execute all papers necessary in connection with any interference which may be declared concerning this application or continuation or division or reissue thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such interference.

3) The undersigned agree to perform all affirmative acts which may be necessay to obtain a grant of valid United States patent to the Assignee.

4) The undersigned agree to communicate to the Assignee or representatives thereof any facts known to us respecting the invention and improvements thereof, and will, upon request, but without expense to us, testify in any legal proceedings regarding the invention.

5) The undersigned hereby authorize and request the Commissioner of Patents to issue any and all Letter Patents the United States resulting form said application or any division or divisions or continuing applications thereof to the said Assignee, as Assignee of the entire interest, and hereby convenant that they have full right to convey the entire interest herein assigned, and that they have not executed and will not execute, any agreement in conflict herewith.

6) The undersigned hereby grant the firm of Glenn Patent Group the power to insert on this assignment any further identification which may be necessary or desirable in order to comply with the rules of the United States Patent Office for recordation of this document.

7) This Agreement shall be binding upon our heirs, executors, administrators, and/or assigns, and shall inure to the benefit of the heirs, executors, administrators, successors and/or assigns of the Assignee.

IN WITNESS WHEREOF, this Assignment was executed by the undersigned on the dates opposite the undersigned names.

Date June 08, 2001 Inventor V. Neumeier Witness .....
NEUMEIER, Karl

Date June 08, 2001 Inventor Dieter Bollmann Witness .....
BOLLMANN, Dieter

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FORM PTO-1619A
Expires 06/30/99
OMB 0651-0027

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Name (line 1): Karl — Execution Date Month Day Year: 6/8/01
Name (line 2): Neumeier

Second Party
Name (line 1): Dieter — Execution Date Month Day Year: 6/8/01
Name (line 2): Bollmann

Receiving Party

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Name (line 2): Der Angewandten Forschung E.V.
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Page 2

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PATENT

Correspondent Name and Address Ar a Cod and Telephone Number 650-474-8400

Name: Michael A. Glenn

Address (line 1): 3475 Edison Way, Suite L

Address (line 2): Menlo Park, CA 94025

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Patent Application Number(s)			Patent Number(s)		
09/868,156					

If this document is being filed together with a new Patent Application, enter the date the patent application was signed by the first named executing inventor. Month Day Year

Patent Cooperation Treaty (PCT)

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Fee Amount Fee Amount for Properties Listed (37 CFR 3.41): $ 40.00

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Statement and Signature

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document. Charges to deposit account are authorized, as indicated herein.

Michael A. Glenn		9/14/01
Name of Person Signing	Signature	Date

Translation

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INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference FH990907PCT	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/EP99/07204	International filing date (*day/month/year*) 29 September 1999 (29.09.99)	Priority date (*day/month/year*) 15 December 1998 (15.12.98)
International Patent Classification (IPC) or national classification and IPC G01L 13/02, 9/12, 9/06, G01P 15/08		
Applicant FRAUNHOFER-GESELLSCHAFT ZUR FÖRDERUNG DER ANGEWANDTEN FORSCHUNG E.V.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 9 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 8 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☒ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
03 July 2000 (03.07.00)	28 March 2001 (28.03.2001)
Name and mailing address of the IPEA/EP Facsimile No.	Authorized officer Telephone No.

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

Inte[redacted]al application No.
PCT/EP99/07204

I. Basis of the report

1. This report has been drawn on the basis of (*Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments.*):

☒ the international application as originally filed.

☒ the description, pages 1,2,4-17, as originally filed,
pages _____, filed with the demand,
pages 3,3A, filed with the letter of 10 January 2001 (10.01.2001),
pages _____, filed with the letter of _____.

☒ the claims, Nos. _____, as originally filed,
Nos. _____, as amended under Article 19,
Nos. _____, filed with the demand,
Nos. 1-15, filed with the letter of 10 January 2001 (10.01.2001),
Nos. _____, filed with the letter of _____.

☒ the drawings, sheets/fig 1/2, 2/2, as originally filed,
sheets/fig _____, filed with the demand,
sheets/fig _____, filed with the letter of _____,
sheets/fig _____, filed with the letter of _____.

2. The amendments have resulted in the cancellation of:

☐ the description, pages _____
☐ the claims, Nos. _____
☐ the drawings, sheets/fig _____

3. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).

4. Additional observations, if necessary:

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/EP99/07204

IV. Lack of unity of invention

1. In response to the invitation to restrict or pay additional fees the applicant has:

- ☐ restricted the claims.
- ☐ paid additional fees.
- ☐ paid additional fees under protest.
- ☐ neither restricted nor paid additional fees.

2. ☐ This Authority found that the requirement of unity of invention is not complied with and chose, according to Rule 68.1, not to invite the applicant to restrict or pay additional fees.

3. This Authority considers that the requirement of unity of invention in accordance with Rules 13.1, 13.2 and 13.3 is

- ☐ complied with.
- ☐ not complied with for the following reasons:

4. Consequently, the following parts of the international application were the subject of international preliminary examination in establishing this report:

- ☐ all parts.
- ☐ the parts relating to claims Nos. _____

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

Continuation of: Box IV.3

In addition to the common preamble, independent Claims 1-4 relate to the following:

- the provision of at least one further intermediate layer between the two wafers. All the intermediate layers are structured so that there is a cavity between the wafers. An opening gives access to this cavity (Claim 1);
- the subdividing of a wafer structure into chips so as to create an opening as per Claim 1 (Claim 2);
- the structuring of an intermediate layer to create two cavities with a connecting channel. An opening is created in the membrane-like structure above one of the cavities (Claim 3);
- the creation of a plurality of openings in the membrane-like structure so as to provide a substrate structure for a mass in an acceleration sensor (Claim 4).

All the technical features of the preamble of these claims are known and published in DE-C-195 43 893 (document D1).

Other common technical features, including the presence of a cavity and an access opening, are also known *per se* and are published in D1 and in US-A-4 586 109 (column 6, lines 13-19).

The remaining special technical features (namely (1) a further structured intermediate layer, (2) openings created by subdividing, (3) two cavities with a connecting channel and an opening above one of the cavities, and (4) the creation of a substrate structure for a mass in the membrane) are not the same or equivalent within the meaning of PCT Rule 13.2.

INTERNATIONAL PR INARY EXAMINATION REPORT

International application No.
PCT/EP 99/07204

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-15	YES
	Claims		NO
Inventive step (IS)	Claims	1-15	YES
	Claims		NO
Industrial applicability (IA)	Claims	1-15	YES
	Claims		NO

2. Citations and explanations

[1] The application discloses a process for manufacturing a microelectromechanical element, wherein according to Claim 1:

(a) a layer on a semiconductor wafer is structured so as to create a recess, and

(b) a second semiconductor wafer is joined to the first so that the recess defines a sealed cavity, and

(c) one of the wafers is thinned so as to create a membrane-like structure above the cavity, and

(d) electronic components are created in the thinned semiconductor wafer, and

(e) a further intermediate layer is provided between the two semiconductor wafers, the said further layer being structured so that it combines with the recess to define a cavity, and
an opening to the cavity is created.

Prior art

DE-C-195 43 893 (document **D1**) discloses (see column 8, line 25 - column 10, line 45, and column 4, line 64 - column 5, line 8; Figures 3a, 4a, 5 and 7) all the above features with the exception of step (e).

Advantage of the invention

The different structuring of the individual layers makes it possible to create cavities with regions of different heights (see the description, page 8, lines 9-13).

Claim 1 meets the requirements of PCT Article 33.

[2] Independent Claim 2 also defines steps (a) to (d) as per Claim 1, and specifies that

(e) at the same time a plurality of microelectromechanical elements is created and then separated, such that the separation (subdivision) creates an opening to the cavity (cavities).

Prior art

Document D1

Advantage of the invention

A simple way to create access openings (see the description, page 11, second paragraph).

Claim 2 meets the requirements of PCT Article 33.

[3] Independent Claim 3 also defines steps (a) to (d) as per Claim 1, and specifies that

(e) the intermediate layer is structured so as to create two cavities and a connecting channel, and an opening is created in the membrane-like structure above one of the cavities.

Prior art

Document D1

Advantage of the invention

Permits use as a differential pressure sensor with pressure connections on one side (see the description, page 14, first paragraph).

Claim 3 meets the requirements of PCT Article 33.

[4] Independent Claim 4 also defines steps (a) to (d) as per Claim 1, and specifies that

(e) a plurality of openings is created in the membrane-like structure so as to provide a substrate structure for a mass in an acceleration sensor.

Prior art

Document D1

Advantage of the invention

Simplified way to manufacture an acceleration sensor (see the description, page 15, third paragraph, and page 16, first paragraph).

Claim 4 meets the requirements of PCT Article 33.

Claims 5-15 are genuine dependent claims and are therefore also novel and inventive.

National Phase of PCT/EP99/07204 in U.S.A.
Title: Method of Producing a Micro-Eletromechanical Element
Applicants: NEUMEIER, Karl; BOLLMANN, Dieter;

Translation of PCT Application PCT/EP99/07204
as originally filed

Method of Producing a Micro-Electromechanical Element

Description

The present invention relates to a method of producing a micro-electromechanical element, and, more specifically, to a micro-electromechanical element which is implemented such that a micromechanical structure and electronic components are arranged in the same semiconductor wafer.

Due to the fast development in the field of semiconductor industry and microelectronics, micromechanical elements, e.g. silicon-based micromechanical pressure measurement cells, replace classical mechanical pressure transducers more and more. Micromechanical elements are used in great amounts e.g. in the fields of automation technology and medical engineering as well as in automotive vehicles. The systems preferably used in this connection are micro-electromechanical integrated systems which realize the combination of mechanical and electronic functions on one substrate. In addition to the electronic components produced in CMOS or similar technologies, which are e.g. measuring transducers, amplifiers, storage means, microcontrollers, etc., mechanical components exist in the same layers. These mechanical components may e.g. be diaphragms of pressure sensors, elastic sheets of valves or pumps, oscillating masses of acceleration sensors, movable fingers or cantilevered arms of switches and the like. In addition to the more or less smooth surface which normally exists in the field of planar technology, these mechanical structures have a three-dimensional structural design and comprise cantilevered structures and buried cavities.

Up to now, it has been known to produce such cavities by wet-chemical etching or by connecting two disks which have been fully processed individually in advance. The techniques which may be used as a connection technique for connecting the individually processed disks are wafer bonding (silicon fusion bonding), anodic bonding or glueing. In any case, the individual disks are fully processed before they are connected in accordance with conventional methods, so that processing steps which may impair the mechanical structures need not be carried out afterwards.

When a wet-chemical undercutting of structures is carried out, the so-called "sticking" problem arises in the case of which the cantilevered structure will adhere to the neighbouring surface due to capillary forces occurring when the liquid dries; hence, the cantilevered structure will lose its movability. Small ditches, holes and gaps additionally cause problems when the structure in question is to be wetted with liquids (e.g. etching solutions, cleaning water, photoresist) and during the removal of these liquids, the problems being then caused e.g. by bubbles which may adhere to the structure in corners thereof. In the case of spinning, drops may remain, which will cause marks when they dry up. Cleaning by means of brushes is problematic as well, since the movable structures may break off during such cleaning processes. A clean surface of the structures is, however, necessary so that the production methods for producing the evaluation structures, such as a CMOS method, can be applied. Due to the risk of carrying over particles and contaminations, the CMOS ability may no longer be given in the case of open structures, i.e. certain sequences of process steps are not allowed in an CMOS line. In addition, when the chips comprised in the wafer are diced by means of a wafer saw, water is used

as a rinsing liquid, which may penetrate into open cavities thus aggravating the particle and contamination problem.

It is additionally known to produce diaphragm-like structures making use of KOH back etching, when the electronic components on the front surface of a wafer have been finished. Due to the oblique etch edges occurring in the case of KOH etching, the integration level will, however, decrease substantially when this method is used, especially when a high number of micro-electromechanical components is produced from one wafer.

Various methods of producing semiconductor pressure sensors are additionally described in DE 3743080 A1.

It is the object of the present invention to provide a method of producing a micro-electromechanical element, which permits the use of conventional standard semiconductor production processes for producing electronic components in the wafer in which micromechanical elements are formed as well, the method permitting the production of micro-electromechanical elements with a high yield.

This object is achieved by a method of producing a micro-electromechanical element according to claim 1.

The present invention provides a method of producing a micro-electromechanical element in the case of which a first intermediate layer, which is applied to a first main surface of a first semiconductor wafer, is structured in a first step so as to produce a recess. The first semiconductor wafer is then connected via the first intermediate layer to a second semiconductor wafer in such a way that a hermetically sealed cavity is defined by the recess. Subsequently, one of the

ity is defined by the recess. Subsequently, one of the wafers is thinned from a surface facing away from the first intermediate layer so as to produce a diaphragm-like structure on top of the cavity. Electronic components are then produced in the thinned semiconductor wafer, preferably by making use of standard semiconductor processes, whereupon at least one defined opening is produced so as to provide access to the hermetically sealed cavity.

It follows that, according to the present invention, the cavity which, together with the diaphragm-like structure, defines a micromechanical element will always remain hermetically sealed until the electronic components, e.g. an integrated circuit, have been finished so that the above-described problems entailed by the use of e.g. an CMOS method for producing an integrated circuit will not arise when the method according to the present invention is used. In addition, due to the hermetically sealed cavity, the above-mentioned problems of removing the etching liquids from the cavities will not arise, since due to the fact that the cavities are hermetically sealed, it is impossible that media, such as liquids, gases, solids and the like, penetrate into the respective cavity during the production of the integrated circuit. It follows that the method according to the present invention permits micro-electromechanical elements, e.g. pressure sensors or controlled valves, to be produced by a reduced number of processing steps so that production at a reasonable price is made possible by the present invention.

According to the present invention, these advantages are achieved in that a hermetically sealed cavity is formed in an intermediate layer which is used for connecting two semiconductor wafers. According to preferred embodiments of the pre-

sent invention, both semiconductor wafers have an intermediate layer applied thereto, one or both of these intermediate layers being structured so as to form the cavity after the connecting step; the intermediate layers are insulating or conductive layers which may consist e.g. of oxide (thermal or TEOS), polysilicon, nitride or metal. These intermediate layers can be interconnected by means of known connection methods, e.g. wafer bonding (silicon fusion bonding), anodic bonding or by means of an adhesive. Alternatively, a larger number of intermediate layers can be used between the wafers to be connected so as to permit the production of a cavity with areas of variable height.

For opening the hermetically sealed cavity, a great number of methods can be used; according to preferred embodiments of the present invention, access to the cavity is realized by producing a defined opening in the diaphragm-like structure, since an access to the cavity can be produced in this way without major effort. The opening in the diaphragm-like structure can be defined by means of a multiplicity of methods, e.g. by making use of a needle or a blade, by making use of a pulsed laser radiation or by means of etching methods. When the method according to the present invention is used for producing in a wafer a plurality of microelectromechanical elements, which are subsequently diced, access to the previously hermetically sealed cavity can be provided by the dicing step; this can be done by structuring a channel when the intermediate layer or the plurality of intermediate layers is being structured, this channel extending up to the boundary surface at which the dicing will be carried out subsequently.

The method according to the present invention is particularly suitable for producing pressure sensors or acceleration sensors; it is, however, also suitable for producing fluid systems which, together with sensors, actors and/or evaluation logics, are realized as a microsystem.

In order to produce a differential pressure sensor, at least two cavities which are hermetically sealed from their surroundings are produced according to the present invention in the intermediate layer or intermediate layers arranged between the wafers, these cavities being interconnected by a channel and the diaphragm-like structure arranged on top of one of these cavities being then provided with an opening so that, via this opening, a pressure can be applied to the lower surface of the unopened diaphragm-like structure, so that the differential pressure between the upper surface and the lower surface of this diaphragm can be detected.

The ratio of the cavity volume to the flow resistance of the connection channel can be varied within wide limits in such a way that the response time, i.e. the time constant, of the sensor will be in a desired range. A variometer for use in aerial navigation can e.g. be realized in this way.

Furthermore, the method according to the present invention is suitable for producing acceleration sensors; in this case, a plurality of openings is realized in the diaphragm-like structure in such a way that the diaphragm-like structure defines a supporting structure for the movable mass.

Further developments of the present invention are specified in the dependent claims.

In the following, preferred embodiments of the present invention will be explained in detail making reference to the drawings enclosed, in which:

Fig.1a) to 1c) show schematic cross-sectional views for explaining an embodiment of the method according to the present invention;

Fig. 2 shows schematically an exploded view for illustrating an embodiment of the method of producing a differential pressure sensor according to the present invention; and

Fig. 3 shows a schematic representation for further explaining the embodiment of the method of producing a differential pressure sensor according to the present invention.

Making reference to Fig. 1, the steps for producing the micromechanical element and the electronic components of a micro-electromechanical element are first described, all the cavities of the micromechanical element being hermetically sealed until the method shown in Fig. 1a) to 1c) has been finished.

As can be seen in Fig. 1a), an intermediate layer 4, which is applied to a first semiconductor wafer 2, is first structured so as to form a recess 6 therein. Subsequently, the semiconductor wafer 2 is connected via the intermediate layer 4 to a second semiconductor wafer 8 which, in the case of the embodiment shown, is also provided with an intermediate layer 10. Due to the connection of the two wafers 2 and 8, a hermetically sealed cavity 12 is defined by the recess 6, as can

be seen in Fig. 1b). When the two wafers 2 and 8 have been connected, the first wafer 2 is thinned from its main surface facing away from the wafer 8 so as to produce a diaphragm-like structure 14 on top of the cavity 12. In the course of this process, the cavity 12 defined in the intermediate layer 4 remains hermetically sealed.

Fig. 1b) shows the micromechanical structure produced; the production method of this micromechanical structure permits integrated circuit structures 16 to be produced in the thinned wafer 2 by means of conventional standard semiconductor processes, the thinned wafer 2 having the diaphragm-like structure 14 formed therein; these integrated circuit structures can be used for evaluating signals that have been produced by the diaphragm 14. The micromechanical structure becomes in this way the micro-electromechanical structure shown in Fig. 1c) in the case of which a semiconductor wafer 2 has formed therein a micromechanically produced diaphragm 14 as well as an integrated circuit 16 which has been produced e.g. by conventional CMOS techniques. The method according to the present invention permits this production of a micro-electromechanical element making use of conventional standard semiconductor production processes, e.g. CMOS processes, since the cavity 12 always remains hermetically sealed until the integrated circuit has been finished. Hence, the present invention permits an economy-priced production of micro-electromechanical elements by means of a - in comparison with conventional methods - reduced number of method steps.

The material used for the semiconductor wafers in the method according to the present invention is preferably silicon, the intermediate layer or the intermediate layers 4 and 10 in Fig. 1 consisting preferably of an oxide, polysilicon, a ni-

tride or metal. In this respect, it should be pointed out that, although an intermediate layer is arranged on both wafers of the above-described embodiment, the method according to the present invention requires only one intermediate layer in which the recess is structured. According to alternative embodiments, a plurality of intermediate layers can be provided between the wafers so that it will be possible to produce cavities with areas of different heights by structuring the individual layers differently. Alternatively to the method shown in Fig. 1, it would also be possible to provide a structure also in the intermediate layer10 applied to the second substrate 8, so that this structure will, together with the structure provided in the intermediate layer 4, define the cavity when the wafers have been connected. Reference should be made to the fact that a quasi-unlimited possibility of structuring intermediate layers for producing different cavities exists as long as the cavities are hermetically sealed after the connection of the two wafers. The structuring for producing these cavities can be carried out by means of known structuring techniques, e.g. photolithography and wet etching or dry etching, or by means of selective deposition.

The wafers can be connected by means of known connection methods; the two wafers are placed one on top of the other such that they are in contact via the connection layer or connection layers, and interconnected by means of special processes, e.g. anodic bonding processes, adhesive processes or the so-called silicon fusion bonding. When this connection has been established, a hermetically sealed cavity 12 is formed by the recess or the recesses which have initially been structured in the intermediate layer or in the intermediate layers, this cavity being shown in Fig. 1b). Subse-

quently, one of the two semiconductor wafers is thinned to a predetermined thickness so that a diaphragm-like structure is formed on top of the cavity. The wafer to be thinned can preferably consist of an SOI material (silicon on insulator), which will facilitate exact thinning. By means of this thinning, a sensor-specific zone or diaphragm is produced on top of the structured areas, i.e. on top of the cavities, whereas the residual area of the thinned wafer can be used for the integration of electronic circuits.

The mechanical structures produced according to this method - one of these structures being shown in Fig. 1b) by way of example - still have a planar surface which is closed at the top and below this surface one or a plurality of hermetically sealed cavities. Hence, the thinned wafer can be processed by the conventional CMOS technologies.

The shape of these hermetically sealed cavities has an arbitrary plan area, in the simplest case rectangular, polygonal or round, and it may comprise elongate and convolute channels or it may consist of a plurality of isolated structures or structures which are connected with channels. The height of the cavities is given by the thickness of the structured layer, as can be seen in Fig. 1a; hence, this height will be uniform in the simplest case. As has already been mentioned hereinbefore, the height of the cavities can, however, be varied in an arbitrary manner by structuring a single layer more than once or by structuring several layers, i.e. cavities with areas of different heights can be produced.

In accordance with preferred embodiments of the method according to the present invention, the step of connecting the two wafers is carried out in a vacuum so that in the case of

high-temperature processes which may perhaps be carried out later on no excess pressure will result from the thermal expansion of a gas contained in the hermetically sealed cavities. This will prevent the diaphragm-like structures produced on top of the cavity or cavities from being damaged, since it is easier to resist e.g. a negative pressure of 1 bar in the cold condition, which exists e.g. in the case of a vacuum in the cavity, than an excess pressure of 3 bar in a diffusion furnace at e.g. 1100°C, when the connection of the wafer does not take place in a vacuum. Depending on the respective use of the micromechanical structure produced according to the present invention it is, however, also possible to fill the cavity with a special gas at an arbitrary pressure.

According to the present invention, at least one defined opening is produced, when the method shown in Fig. 1a) to 1c) has been finished, so as to provide access to the hermetically sealed cavity. A differential pressure sensor or, alternatively, an acceleration sensor can thus be realized by the element shown in Fig. 1c), when the openings in the diaphragm-like area 14 are e.g. defined in such a way that they define a supporting structure for a movable mass.

When the method steps shown in Fig. 1a) to 1c) have been finished, the cavity or the cavities according to the present invention are opened at predetermined locations. This opening of the cavities can take place in a vacuum chamber, in the ambient air, in a protective gas, in a special atmosphere or under a liquid. In any case, the medium in question will penetrate into the cavity and fill it completely, when the cavity was under a vacuum before, i.e. when the wafer-

connecting step has taken place in a vacuum, as has been explained hereinbefore.

The opening of the cavity can be realized in different ways. For producing a differential pressure sensor, which production will be explained in detail in the following making reference to Fig. 2 and 3, the diaphragm-like structure arranged on top of one of the cavities can e.g. be opened by puncturing by means of a needle or a blade. In order to prevent the fragments which are likely to be produced from penetrating into neighbouring cavities, the channels interconnecting the cavities may be implemented after the fashion of a labyrinth. Alternatively, it is also possible to open the diaphragm-like structure on top of one of the cavities by means of a pulsed laser radiation. In the case of this method fragments and possible microcracks are avoided so that the reliability will not be endangered. Furthermore, the vapours and molten droplets produced can be rendered harmless by providing the channels with a suitable structural design. These two methods for opening the cavities are suitable for chips which have already been sawn, diced and perhaps mounted in a housing. When the cavities have been opened, the tubules used for connection to the pressure-carrying medium are mounted when the component in question is a pressure sensor.

Normally, a plurality of micro-electromechanical elements are formed in a wafer, which are then diced so as to obtain individual chips. The opening of the cavities can then take place during the sawing of the wafers, when the channels have been implemented such that they extend down to the scratch frame defining the saw paths. The channels are then accessible from the lateral surfaces of the chips, and this can be advantageous for the mounting operation. The ingress of cooling wa-

ter can be avoided by dry sawing, by scribing and breaking or by cutting with pulsed laser radiation.

The cavities can also be opened by purposeful etching, e.g. in a plasma etcher. In this case, the surface of the wafer and, consequently, the diaphragm-like structure have applied thereto a protective layer, e.g. a passivation layer or a photoresist, which is has apertures at the locations at which the opening or the openings are to be formed. At these locations the diaphragm is etched away, whereas it is preserved at the protected locations. In contrast to liquids, the gas penetrating in the course of this process does not cause any problems in the cavities. The passivation can remain on the component after this etching step, whereas the photoresist can be removed by incineration in plasma. This etching method can be carried out prior to dicing of the chips for a plurality of elements comprised in the wafer or after the dicing of the chips.

Making reference to Fig. 2 and 3, a preferred embodiment of the method of producing a differential pressure sensor according to the present invention will be described in the following. Micromechanically integrated pressure sensors measure an externally applied pressure of a gas or of a liquid and process this pressure so as to obtain an electric signal. Normally, these sensors are implemented as absolute pressure sensors. Such a sensor may e.g. have the structural design shown in Fig. 1c), in the case of which a thin layer is located on top of a hermetically sealed cavity, this layer acting after the principle of an aneroid barometer as a diaphragm. In order to be as independent as possible of temperature variations of the surroundings, the cavity is normally empty, i.e. it is under a vacuum.

Frequently, it is desired to compare the pressure of two volumes; in this case, only the pressure difference is of interest. The pressure difference to be measured is often very small in comparison with the absolute pressure. Hence, the measuring accuracy would be very low if the measurement were carried out by forming the difference between the measured values of two absolute pressure sensors. It will be more advantageous to connect the diaphragm on either side thereof to the volumes to be measured and to measure only the pressure difference. In the case of macroscopic sensors with diaphragms of metal or rubber such a sensor can be realized easily. In the case of microelectronically integrated sensors, however, the two sides of the diaphragm are no longer symmetrical. In planar technology there is always an upper side which is exposed to the technological processes and which is easy to clean and a lower side which is protected against aggressive gases and liquids during the production process. In order to permit the wafers to be processed by conventional standard semiconductor processes, e.g. CMOS technologies, they must have a planar surface which is closed at the top. This is made possible by the method according to the present invention, this method permitting thus micromechanical elements and electronic components, which have been formed making use of conventional semiconductor processes, to be integrated in a wafer.

As can be seen in the schematic exploded view of Fig. 2, two cavities 20 and 22 are produced in an intermediate layer 24, which is formed between two wafers 26 and 28, so as to produce a differential pressure sensor. The two cavities are interconnected by a channel 30 which is defined in the intermediate layer 24. It is evident that Fig. 2 shows the state of

the process which is shown in Fig. 1b) for a single cavity, the upper wafer 26 being shown separately from the intermediate layer 24 only for the sake of clarity, so that the cavities 20 and 22 as well as the channel 30 formed in the intermediate layer 24 are hermetically sealed from the surroundings. In this connection, it should also be pointed out that the cavities and the channel may also be structured in plurality of intermediate layers so as to be able to define areas of different heights or so as to produce predetermined breaking points for the future opening step.

In the schematic representation of Fig. 2, the upper wafer 26 has already been thinned so that diaphragm-like structures 32 and 34, Fig. 3, are formed on top of the cavities 20 and 22, the outlines of these diaphragm-like structures being indicated by broken lines in Fig. 3. When the structure shown in Fig. 2 has been produced, the diaphragm 34 arranged on top of the cavity 22 has formed on opening 36 therein, which defines an access to the cavity 22 and, consequently, via the channel 30 also to the cavity 20. In this connection, it should be pointed out that the opening is not formed in the diaphragm 34 until the semiconductor production, i.e. the production of electronic components, e.g. in the form of an evaluation unit, in the semiconductor wafer 26 has been finished. For this semiconductor production conventional standard semiconductor processes, e.g. CMOS processes, can be used, since all the cavities are hermetically sealed at the time of the semiconductor production. Furthermore, reference should be made to the fact that the electronic components are not shown in Fig. 3.

The micromechanical element shown in Fig. 3 can serve as a differential pressure sensor, since a first pressure can act

on the upper surface of the diaphragm 32, whereas a second pressure can act on the lower surface thereof via the opening 36, the cavity 22, the channel 30 and the cavity 20 so that the output signal of the sensor defined by the diaphragm 32 and the cavity 20 will be representative of the difference between these two pressures. In order to permit this, the build-up and connection technique can comprise the step of connecting the sensor, i.e. the diaphragm 32 and the open second cavity 22, to a respective gas volume e.g. by means of glued-on small tubes. Since the second cavity 22 communicates through the channel 30 with the lower surface of the diaphragm 32 through gas exchange, the pressure applied here acts on the lower surface of the diaphragm 32. Hence, the sensor will register the differential pressure between the two connections. Both connections can be mounted from the upper side of the sensor, whereby the structural design can be simplified.

Alternatively, it is possible to implement the pressure sensor, which is defined by the diaphragm 32 and the cavity 20, as well as the channel and the second cavity several times so as to produce e.g. a sensor array. The ratio of the cavity volume to the flow resistance of the connection channel can be varied within wide limits so that the sensor response time can be adjusted.

In addition to the above-described use of the method according to the present invention for producing differential pressure sensors, the method according to the present invention is also suitable for producing mechanically oscillatory sensors and actors; also in the case of these components it will be advantageous when the sensor and the associated evaluation electronics are integrated on the same chip. Such mechani-

cally oscillatory sensors and actors are required e.g. in airbag trigger devices, accelerometers, tuning forks, rotary encoders, valves, pumps, switches and the like. A special feature required in this connection is an oscillating mass which is suspended from comparatively thin holders. These holder serve as elastic springs.

According to the present invention, such a holding structure for a movable mass can be produced e.g. by taking as a basis the structure which has been described as pressure sensor in Fig. 1c) and by providing the diaphragm-like area 14 with openings so as to define such a supporting structure. In this connection, it should be pointed out that during the semiconductor production, i.e. during the production of the evaluation circuit, a movable mass is attached to the diaphragm 14 or formed in this diaphragm 14 by structuring. It is obvious that the evaluation circuit shown in Fig. 1c) as an evaluation circuit 16 for a pressure sensor will have to be adapted to an acceleration sensor in a suitable manner. During the semiconductor production, the diaphragm-like area is completely connected to the surrounding area of the wafer in which the diaphragm-like area is formed so that the cavity below the diaphragm-like area is hermetically sealed.

As has already been explained hereinbefore, this method provides substantial advantages in the production process with respect to yield, mechanical robustness as well as protection against liquids. In order to make the mass movable at the end of the semiconductor production process in which the electronic components are produced, the diaphragm is removed at the boundary of the mass preferably by means of an etching process. The part of the diaphragm which is intended to be used as a holder is protected against the attack of the

etchant and is preserved. In comparison with the above-mentioned openings, e.g. of the cavity 22 in the case of the differential pressure sensor shown in Fig. 2 and 3, the surface to be etched is large in the case of this application. Since the movable mass should be as big as possible, it will be advantageous to make it as thick as possible. Since the areas to be opened should, on the other hand, have the thinnest possible diaphragms so that they can be opened easily, it will be advantageous to structure a plurality of layers in different ways. This requires respective additional lithographic planes. The oscillating mass, which is obtained by the supporting structure produced in the manner described hereinbefore, can be produced from a multi-layer structure consisting of silicon, metal or oxide.

A further field of application which should be mentioned in connection with the method for producing micro-electromechanical structures according to the present invention are fluid systems. The chemical reaction vessels realized in macroscopic systems by glass tubes, glass bulbs as well as rubber hoses are implemented in a miniaturized form in silicon or in some other material which is suitable for microsystem technology in microfluid systems. The use comprises the dosage, mixing and physical measurement of small amounts of liquid and of the chemical and biological reactions thereof. The cavities, their connection channels as well as branches and connection openings are structured in one or in a plurality of intermediate layers, which are arranged between two wafers, according to the present invention. The cavities are then hermetically sealed by subsequently connecting the wafers, whereupon one of the wafers is thinned. This wafer has a planar upper surface and is therefore adapted to be processed by the conventional CMOS tech-

nologies so that electronic sensors, such as pressure sensors, temperature sensors, conductivity sensors or also photodiodes for light absorption, and actors, e.g. amplifiers, microcontrollers, electrodes and the like, can be built up in the immediate vicinity of the vessels. This integration of sensor, actor and logic on a substrate makes the component a microsystem. When the semiconductor production has been finished, the cavities provided for connection are opened at predetermined locations in accordance with the above-described methods and connected to the supply lines feeding the liquid.

It follows that the present invention permits the production of micro-electromechanical elements in the case of which all the cavities of the micromechanical structures of these micro-electromechanical elements are hermetically sealed after their production, and a planar surface which is closed at the top is provided so that the wafers can be processed from above making use of conventional CMOS technologies. The cavities are not opened until the electronic components have been finished. Problems entailed by conventional methods due to the cleaning of wafer surfaces and the ingress of liquids into cavities as well as due to the carrying over of particles and contaminations are therefore eliminated by the method according to the present invention. Hence, the present invention provides a method which requires little expenditure and which permits the production of micro-electromechanical elements at a reasonable price and with a high yield.

Claims

1. A method of producing a micro-electromechanical element comprising the following steps:

a) structuring a first intermediate layer (4; 24), which is applied to a first main surface of a first semiconductor wafer (2; 26), so as to produce a recess (6; 20, 22, 30);

b) connecting the first semiconductor wafer (2; 26) via the first intermediate layer (4; 24) to a second semiconductor wafer (8; 28) in such a way that a hermetically sealed cavity (12; 20, 22, 30) is defined by the recess;

c) thinning one of the wafers (2; 26) from a surface facing away from said first intermediate layer (4; 24) so as to produce a diaphragm-like structure (14; 32, 36) on top of the cavity (12; 20, 22);

d) producing electronic components (16) in said thinned semiconductor wafer (2; 26);

e) producing at least one defined opening (36) so as to provide access to the hermetically sealed cavity (20, 22).

2. A method according to claim 1, wherein the main surface of the second semiconductor wafer (8), which is connected to the first semiconductor wafer (2) via the in-

termediate layer (4), has applied thereto a second intermediate layer (10) prior to the connecting step.

3. A method according to claim 2, wherein the second intermediate layer is structured in such a way that, after the connecting step, the structure formed in the second intermediate layer and the recess in the first intermediate layer define the cavity.

4. A method according to one of the claims 1 to 3, wherein, in addition to the first intermediate layer, further intermediate layers are provided between the two semiconductor wafers, said intermediate layers being structured before the two semiconductor wafers are connected, so as to produce a cavity with areas of variable height.

5. A method according to one of the claims 1 to 4, wherein the first and the second wafer (2, 8; 26, 28) consist of silicon.

6. A method according to one of the claims 1 to 5, wherein said one or said plurality of intermediate layers consist(s) of an oxide, a polysilicon, a nitride or of metal.

7. A method according to one of the claims 1 to 6, wherein said one or said plurality of intermediate layers (24) are structured in such a way that, after the connection of the two wafers (26, 28), a plurality of cavities (20, 22) is defined, said cavities being interconnected by channels (30) and hermetically sealed from their surroundings.

8. A method according to one of the claims 1 to 7, wherein the connection in step b) is carried out in a vacuum.

9. A method according to one of the claims 1 to 11, wherein an SOI wafer is used as a first (2; 26) and/or second (8; 28) wafer.

10. A method according to one of the claims 1 to 9, wherein said at least one defined opening (36) is produced in the diaphragm-like structure (34).

11. A method according to claim 10, wherein said at least one defined opening (36) is produced in the diaphragm-like structure (34) by means of a needle, a blade, by the use of a pulsed laser radiation or by etching.

12. A method according to one of the claims 1 to 9, wherein a plurality of micro-electromechanical structures is produced in a wafer, said method comprising in addition the step of dicing the individual micromechanical structures so as to obtain chips, said at least one defined opening, which provides access to the hermetically sealed cavity, being produced by the dicing step.

13. A method according to one of the claims 1 to 12, wherein said one or said plurality of intermediate layers (24) is/are structured in step a) in such a way that, after the connection of the two wafers (26, 28), at least two hermetically sealed cavities (20, 22) interconnected by a channel (30) are defined, a diaphragm-like structure (32, 34) being arranged on top of each of said cavities (20, 22) after step c), and a defined opening (36)

through said diaphragm-like structure (34) of one of the cavities (22) being produced in step e).

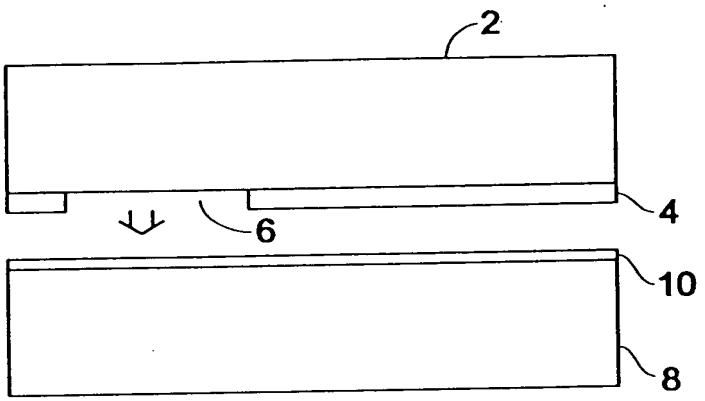
14. A method according to claim 13, wherein the channel is structured in the fashion of a labyrinth in step a) in such a way that disturbing products formed during the production of the opening are prevented from passing said channel.

15. A method according to one of the claims 1 to 12, wherein a plurality of defined openings is produced in the diaphragm-like structure in step e) in such a way that, after the production of the openings, the diaphragm-like structure forms a supporting structure for the movable mass of an acceleration sensor.

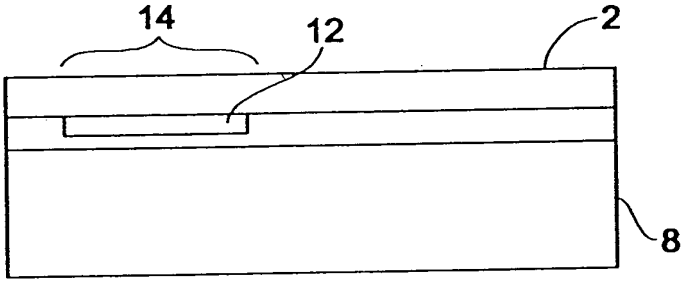
Method of Producing a Micro-Electromechanical Element

Abstract

In a method of producing a micro-electromechanical element a first intermediate layer (4; 24), which is applied to a first main surface of a first semiconductor wafer (2; 26), is structured in a first step so as to produce a recess (6; 20, 22, 30). The first semiconductor wafer (2; 26) is connected via the first intermediate layer (4; 24) to a second semiconductor wafer (8; 28) in such a way that a hermetically sealed cavity (12; 20, 22) is defined by the recess. When one of the wafers (2; 26) has been thinned from a surface facing away from said first intermediate layer (4; 24) so as to produce a diaphragm-like structure (14; 32, 36) on top of the cavity, electronic components are produced in said thinned semiconductor wafer making use of standard semiconductor processes. Finally at least one defined opening (36) is produced so as to provide access to the hermetically sealed cavity (12; 20, 22, 30).



a)



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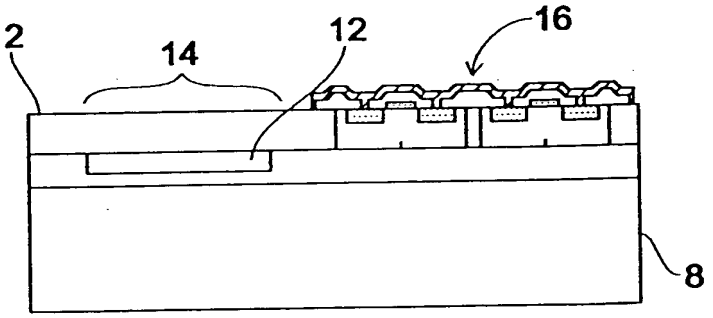

c)

Fig. 1

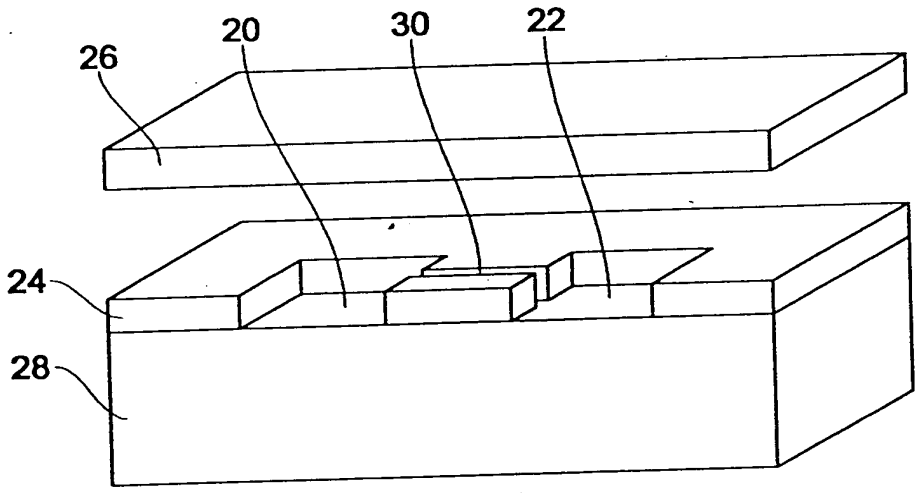

Fig. 2

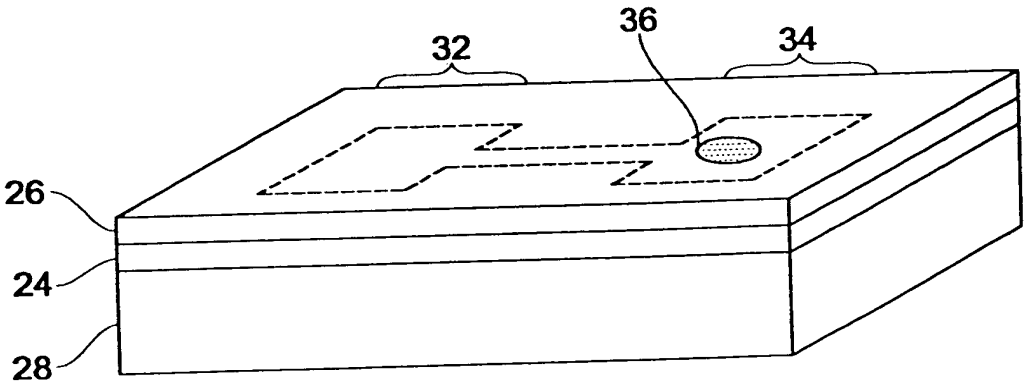

Fig. 3